

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A substrate panel for use in semiconductor packaging, comprising:

a lead-frame panel, including

an array of device areas, each device area having a plurality of contacts exposed on a bottom surface of the substrate panel;[[.]]

a plurality of wire bonding landings exposed on a top surface of the substrate panel;[[.]]

a plurality of electrical contacts arranged so that at least some of the contacts extend through the substrate having an exposed bottom surface on the bottom surface of the substrate; and

lead segments that electrically couple ~~coupling~~ selected wire bonding landings to associated electrical contacts; and

a dielectric material that fills spaces between adjacent lead segments, wherein a top surface of the dielectric material is substantially coplanar with the top surface of the substrate panel and the wire bonding landings, and the bottom surface of the dielectric material is substantially coplanar with the bottom surface of the substrate panel and the electrical lead contacts, thereby forming a substrate panel having substantially planar top and bottom surfaces.

2. (Canceled)

3. (Currently Amended) A substrate panel as recited in claim 1 wherein the wire bonding landings are thinner than the substrate panel, such that the wire bonding landings are not exposed on the bottom surface of the substrate panel and wherein the dielectric material of the substrate is formed underneath the landings to give support to the wire bonding landings said support being sufficient to structurally reinforce the landings during a wire bond process.

4. **(Original)** A substrate panel as recited in claim 1 wherein at least selected portions of the lead segments are thinner than the substrate panel such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate panel.
5. **(Previously Presented)** A substrate panel as recited in claim 1 wherein the device areas are arranged in at least one two dimensional array such that the substrate has at least one two-dimensional array of device areas.
6. **(Previously Presented)** A substrate panel as recited in claim 5 wherein the lead-frame further comprises a matrix of tie bars, the tie bars being positioned between immediately adjacent device areas in the two dimensional array of device areas and configured to support the lead segments.
7. **(Original)** A substrate panel as recited in claim 1 wherein each device area further includes a die attach pad, the die attach pad being exposed on the top surface of the substrate panel.
8. **(Original)** A substrate panel as recited in claim 7 wherein the die attach pad has a plurality of posts exposed on the bottom surface of the substrate panel.
9. **(Currently Amended)** A substrate panel as recited in claim 7 wherein at least one of the wire bonding landings is directly electrically coupled to the die attach pad by a ~~only-an~~ ~~additional~~ lead segment.
10. **(Currently Amended)** A substrate panel as recited in claim 7 wherein ~~the~~ said associated contacts are located closer to the die attach pad than ~~their-associated~~ said selected wire bonding landings.
11. **(Currently Amended)** A substrate panel for use in semiconductor packaging, comprising:

a lead-frame panel including a two dimensional array of device areas, each device area having,

a plurality of contacts exposed on a bottom surface of the substrate panel wherein the contacts are arranged in a microarray configuration.

a plurality of wire bonding landings exposed on a top surface of the substrate panel, and

lead segments configured to electrically couple ~~coupling~~ selected wire bonding landings to associated contacts; and

a dielectric material that fills spaces between adjacent lead segments and underlies at least a portion of each of the wire bonding landings, wherein a top surface of the dielectric material is substantially coplanar with the top surface of the substrate panel and the wire bonding landings, and a bottom surface of the dielectric material is substantially coplanar with the bottom surface of the substrate panel and the lead contacts; and

wherein at least some of the wire bonding landings are thinner than the substrate panel, such that the thinner wire bonding landings are not exposed on the bottom surface of the substrate panel, and at least selected portions of the lead segments are thinner than the substrate panel such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate panel.

12. (Original) A substrate panel as recited in claim 11 wherein each device area further includes a die attach pad, the die attach pad being exposed on the top surface of the substrate panel.

13. (Currently Amended) A substrate panel as recited in claim 12 wherein the contacts surround the die attach pad, and wherein the die attach pad has a plurality of posts exposed on the bottom surface of the substrate panel, the contacts and the posts being arranged in a two dimensional ~~array~~ microarray of rows and columns each comprised of at least one of the contacts and rows.

14. (Currently Amended) A substrate panel as recited in claim 12 wherein at least one of the wire bonding landings is directly electrically coupled to the die attach pad by at least on of the ~~only an additional~~ lead segments.

15. (Currently Amended) A singulated packaged integrated circuit, comprising:

a substrate including a plurality of contacts configured for electrical contact underneath the substrate with the contacts having exposed contact surfaces on a bottom surface of the substrate, a plurality of wire bonding landings at exposed on a top surface of the substrate, lead segments electrically coupling the wire bonding landings to associated ~~lead~~ contacts, and a first dielectric layer that fills spaces between adjacent lead segments and fills space under the wire bonding landings, wherein a top surface of the dielectric layer is substantially coplanar with the top surface of the substrate and the wire bonding landings, and a bottom surface of the dielectric layer that is substantially coplanar with the bottom surface of the substrate panel and substantially coplanar with said contact surfaces ~~the lead contacts~~, thereby forming a substrate having substantially planar top and bottom surfaces;

a die mounted on the substrate, the die having a plurality of bond pads configured for electrical connection to the wire bonding landings;

a plurality of connectors for electrically connecting the plurality of bond pads to associated wire bonding landings; and

a second dielectric layer that encapsulates the die and the plurality of connectors and covers at least a portion of the top surface of the substrate.

16. (Previously Presented) A packaged integrated circuit as recited in claim 15 wherein the first and second dielectric layers are formed from substantially the same materials but are not integrally formed.

17. (Canceled)

18. (Original) A packaged integrated circuit as recited in claim 15 wherein the wire bonding landings are thinner than the thickness of the substrate, such that the wire bonding landings are not exposed on the bottom surface of the substrate.

19. (Original) A packaged integrated circuit as recited in claim 15 wherein at least selected portions of the lead segments are thinner than the thickness of the lead-frame, such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate.

20. (Original) A packaged integrated circuit as recited in claim 15 wherein the substrate further includes a die attach pad surrounded by the lead contacts, the die attach pad being exposed on the top surface of the substrate.

21. (Original) A packaged integrated circuit as recited in claim 20 wherein the die attach pad has a plurality of posts that are exposed on the bottom surface of the substrate.

22. (Currently Amended) A packaged integrated circuit as recited in claim 20 wherein at least one of the wire bonding landings is directly electrically coupled to the die attach pad by a ~~only an additional~~ lead segment.

23. (Original) A packaged integrated circuit as recited in claim 20 wherein at least one of the contacts is located between the wire bonding landings and the die attach pad.

Claims 24 – 30 (Canceled)

31. (Previously Presented) A substrate panel as recited in claim 11 wherein the wire bonding landings are located radially further from a center of their associated device area than their associated contacts and wherein the substrate panel has substantially planar top and bottom surfaces with the wire bond landings and the lead segments being exposed on the top surface of the substrate but not the bottom surface of the substrate.

32. (Previously Presented) A substrate panel as recited in claim 1 wherein at least some of the wire bonding landings have a width that is wider than an immediately adjacent portion of their associated lead segments and a thickness that is substantially the same as their associated lead segments.

33. (Currently Amended) A substrate panel as recited in claim 11 wherein at least some of the wire bonding landings have a width that is wider than an immediately adjacent portion of their associated lead segments and a thickness that is substantially the same as their associated lead segments wherein the increased width of said wire bonding landings facilitates wire bonding to said landings.

34 (Canceled).

35. (Previously Presented) A packaged integrated circuit as recited in claim 15 wherein the package is a leadframe based microarray package.

36. (New) A substrate panel as recited in claim 1 wherein the plurality of contacts exposed on a bottom surface of the substrate panel are arranged in a microarray configuration.

37. (New) A substrate panel as recited in claim 36 wherein the plurality of contacts arranged as a microarray are patterned in a ball grid array (BGA) configuration .

38. (New) A substrate panel as recited in claim 8 wherein the plurality of contacts and the plurality of posts exposed on the bottom surface of the substrate panel are arranged in a micro array.

39. (New) A substrate panel as recited in claim 38 wherein the contacts and posts on the bottom surface of the substrate panel are arranged in a BGA pattern.

40. (New) A substrate panel as recited in claim 11 wherein at least one of the wire bonding landings includes a support footing that extends downward from the bottom surface of said wire bonding landings, the footing configured to support the landing during a wirebonding process and having an exposed surface that is substantially coplanar with the bottom surface of the substrate panel.

41. (New) A substrate panel as recited in claim 15 wherein at least one of the wire bonding landings includes a support footing that extends downward from the bottom surface of said wire bonding landings, each footing configured to support the landing during a wirebonding process and configured to have an exposed surface that is substantially coplanar with the bottom surface of the substrate panel.